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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,253	06/17/2005	Andreas Przadka	14219-075US1/P2002,0539 U	8747

26161 7590 01/19/2007
FISH & RICHARDSON PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
RODELA, EDUARDO A	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,253	PRZADKA, ANDREAS	
	Examiner	Art Unit	
	Eduardo A. Rodela	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed September 11, 2006.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear as to what sort of a device a "ceramic microwave filter" is referring to.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 10, 16, 22, 23, 25, 26, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325).

Regarding claim 1, Fukuoka shows (e.g. Figure 8) an electronic component comprising:

a multi-layer substrate [101] having an upper side and under side, the multi-layer substrate comprising at least one integrated impedance converter [202b]; and at least one chip component [202a] comprising external contacts [206], the at least one chip

component being disposed on the upper side of the multi-layer substrate, the at least one chip component being electrically connected to the at least one integrated impedance converter [202a connects to 202b, through terminal 211 by solder 108 to conductive pattern 109 through substrate wiring 104 to conductive pattern 105 then to wire 210 to pad 206 on chip 202a]. Fukuoka does not specify the function of the at least one integrated impedance converter being configured to perform impedance conversion between different standard impedance levels. Uchida shows (e.g. Figure 1b) an impedance converter [16] being configured to perform impedance conversion between different standard impedance levels [column 1: lines 12-20, 26-33, and 36-42]. Uchida teaches the benefits of an impedance converter being configured to perform impedance conversion between different standard impedance levels to prevent signal reflection to the IC device [column 1: lines 12-20, 26-33, and 36-42] as suggested by Uchida. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to have included an impedance converter being configured to perform impedance conversion between different standard impedance levels in the invention of Fukuoka as suggested by Uchida in order to prevent signal reflection to the IC device.

Regarding claim 2, Fukuoka and Uchida disclose the electronic component of claim 1. In addition Fukuoka shows (e.g. Figure 11) wherein the external contacts [307a] comprise surface mounted device contacts [307a attach to surface pads 306a by 310].

Regarding claim 3, Fukuoka and Uchida disclose the electronic component of claim 1. In addition Fukuoka shows (e.g. Figure 8) wherein the multi-layer substrate comprises, at least one passive circuit element [202b].

Regarding claim 10, Fukuoka and Uchida disclose the electronic component of claim 1. In addition Fukuoka shows (e.g. Figure 8) wherein the at least one discrete circuit element [202b] disposed on the upper side of the multi-layer substrate [101], the at least on discrete circuit element comprising an active circuit element or a passive circuit element [column 16, lines 55-60].

Regarding claim 16, Fukuoka and Uchida disclose the electronic component of claim 1. In addition Fukuoka shows (e.g. Figure 8) wherein the multi-layer substrate [101] comprises ceramic layers [column 16: line 55-60].

Regarding claim 22, Fukuoka and Uchida disclose the electronic component of claim 10. In addition Fukuoka shows (e.g. Figures 8 and 11) wherein the at least one chip component [307] and the at least one discrete circuit element [202b] comprise surface mounted design elements.

Regarding claim 23, Fukuoka and Uchida disclose the electronic component of claim 1. In addition Fukuoka shows (e.g. Figure 8) wherein the at least one chip component [202a] comprises a housing [103] comprising external contacts [109].

Regarding claim 25, Fukuoka and Uchida disclose the electronic component of claim 1. In addition Fukuoka shows (e.g. Figure 11) wherein the at least one chip component [202a] is connected to the multi-layer substrate [101] via flip-chip technology.

Regarding claim 26, Fukuoka shows (e.g. Figure 8) a method of producing an electronic component comprised of a multi-layer substrate [101] having an upper side and under side, the multi-layer substrate comprising at least one integrated impedance converter [202b], and at least one chip component comprising external contacts [211], the method comprising installing the at least one chip [202a] component in a housing [103]; and mounting the housing onto the upper side of the multi-layer substrate [101] so as to electrically connect the at least one chip component to the integrated impedance converter [202a connects to 202b, through terminal 211 by solder 108 to conductive pattern 109 through substrate wiring 104 to conductive pattern 105 then to wire 210 to pad 206 on chip 202a]. Fukuoka does not specify wherein the at least one integrated impedance converter is configured to perform impedance conversion between different standard impedance levels. Uchida shows (e.g. Figure 1b) an impedance converter [16] being configured to perform impedance conversion between different standard impedance levels [column 1: lines 12-20, 26-33, and 36-42]. Uchida teaches the benefits of an impedance converter being configured to perform impedance conversion between different standard impedance levels to prevent signal reflection to the IC device [column 1: lines 12-20, 26-33, and 36-42] as suggested by Uchida. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to have included an impedance converter being configured to perform impedance conversion between different standard impedance levels in the invention of Fukuoka as suggested by Uchida in order to prevent signal reflection to the IC device.

Regarding claim 27, Fukuoka and Uchida disclose the method of claim 26. In addition, Fukuoka show (e.g. Figure 8) further comprising: mounting at least one discrete circuit element [202b] on the upper side of the multi-layer substrate [101].

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Chakravorty (US 6,970,362).

Regarding claim 4, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not disclose wherein the at least one chip component comprising at least one filter circuit. Chakravorty does disclose in Figure 2, a multilayer substrate [55] with a die [40], surface mounted on the upper surface, wherein the at least one chip component comprising at least one filter circuit [column 3, lines 60-67]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made that the chip component of Fukuoka and Uchida could have any sort of circuit therein such as a filter circuit of Chakravorty, in order to further provide functionality to the overall device such as a high frequency filter for a cell phone.

Claims 5, 11, 12, 13, 15, 19, 20, 21, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Uchikoba (US 6,628,178).

Regarding claim 5, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not disclose wherein the at least one chip component comprises at least one resonator that operates with surface acoustic waves. Uchikoba does disclose in Figure 1, a multilayer substrate [40] with a die [30], surface mounted

[face down with connections 31 and 43] on the upper surface of the substrate [40], wherein the at least one chip component [30] comprises at least one resonator that operates with surface acoustic waves [column 7, lines 19-34]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a surface mountable surface acoustic wave device of Uchikoba on the substrate of Fukuoka and Uchida, in order to further provide components necessary for a high frequency filter.

Regarding claim 11, Fukuoka and Uchida disclose the electronic component of claim 10. Fukuoka and Uchida do not disclose wherein the at least one discrete circuit element comprises at least one of the following: a high-frequency circuit, an adjustment circuit, an impedance converter, etc. Uchikoba does disclose in Figures 9-11, wherein the at least one discrete circuit element [15] comprises at least one of the following: an antenna circuit, a diplexer, a low pass filter, and a band pass filter [column 1, lines 52-67]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use the discrete components of Uchikoba on the substrate of Fukuoka and Uchida, in order to further provide components necessary for several types of circuits used in high frequency device applications.

Regarding claim 12, Fukuoka and Uchida disclose the electronic component of claim 10. Fukuoka and Uchida do not show wherein the at least one discrete circuit element comprises at least part of a high-frequency circuit, a duplexer or a diplexer, and wherein the at least on discrete circuit element assists in connecting the at least one chip component to an antenna. Uchikoba discloses in Figures 9-11, wherein the at

least one discrete circuit element [15] comprises at least part of a diplexer [column 1, lines 52-67], and wherein the at least on discrete circuit element assists in connecting the at least one chip component to an antenna [column 1, lines 53-67]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use the discrete components of Uchikoba on the substrate of Fukuoka and Uchida, in order to further provide components necessary for several types of circuits used in high frequency device applications.

Regarding claim 13, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not disclose further comprising: at least one circuit element integrated in the multi-layer substrate; wherein the at least one circuit element comprises at least part of one of the following: a high frequency circuit, an adjustment circuit, an antenna circuit, a diode circuit, etc. Uchikoba does disclose in Figures9-11, a low pass filter, a band pass filter, a diplexer [column 1, lines 53-67]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use the circuit components of Uchikoba on the substrate of Fukuoka and Uchida, in order to further provide components necessary for several types of circuits used in high frequency device applications.

Regarding claim 15, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not show wherein the multi-layer substrate comprises a plurality of adjustment circuits. Uchikoba does disclose in Figures 9-11, wherein the multi-layer substrate [1] comprises a plurality of adjustment circuits [LPF,DPX,BPF]. It would have been obvious to one of ordinary skill in the art at the time that the invention

was made to use the circuit components of Uchikoba on the substrate of Fukuoka and Uchida, in order to further provide components necessary for several types of circuits used in high frequency device applications.

Regarding claim 19, Fukuoka and Uchida discloses the electronic component of claim 1. Fukuoka and Uchida does not specify wherein the at least one chip comprises at least one or more inputs and outputs; and wherein at least one input and/or at least one output of the at least one chip component conducts an asymmetrical signal. Uchikoba does disclose in Figures 9-11, wherein the at least one chip [15] comprises at least one or more inputs and outputs [inherently any operational device would]; and wherein at least one input and/or at least one output of the at least one chip component conducts an asymmetrical signal [components in the LPF and BPF would handle signals with a spectrum of frequencies]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to have the asymmetrical signal handling components of Uchikoba in the device of Fukuoka and Uchida, in order to further provide components necessary for filter circuits.

Regarding claim 20, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not disclose wherein the at least one chip component comprises at least one or more inputs and outputs; and wherein at least one input and/or at least one output of the at least one chip component conducts a symmetrical signal. Uchikoba does disclose wherein the at least one chip component comprises at least one or more inputs and outputs [inherently any operational device would]; and wherein at least one input and/or at least one output of the at least one chip component

conducts a symmetrical signal [Fig. 9: the receiving circuit would have a clock signal, which is symmetrical]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to have the symmetrical signal handling components of Uchikoba in the device of Fukuoka and Uchida, in order to further provide components necessary for a receiver circuit.

Regarding claim 21, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not specify wherein the at least one chip component comprises a connection to ground, the connection to ground being made via an adjustment circuit that is at least partially integrally integrated in the multi-layer substrate; and wherein the adjustment circuit comprises at least one of a coil, a capacitor, and a conductor. Uchikoba does show in Figure 3 of which schematic components are all situated on the ceramic substrate, wherein the at least one chip component [downward facing diode] comprises a connection to ground [schematic ground], the connection to ground being made via an adjustment circuit [parallel resistor and capacitor both connected to ground] that is at least partially integrally integrated in the multi-layer substrate [all schematic components are on the surface of the ceramic capacitor]; and wherein the adjustment circuit comprises a capacitor [capacitor in parallel with resistor both connected to ground] and a conductor. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to have the components in the specified configuration of Uchikoba in the device of Fukuoka and Uchida, in order to further provide the necessary connections to the complex circuits used in high frequency device applications.

Regarding claim 28, Fukuoka and Uchida disclose the method of claim 27. Fukuoka and Uchida do not show wherein the at least one chip component and the at least one discrete circuit element are attached to the upper side of the multi-layer substrate using a same attaching mechanism. Uchikoba does disclose in Figure 1, wherein the at least one chip component [30] and the at least one discrete circuit element [50] are attached to the upper side of the multi-layer substrate [40] using a same attaching mechanism [surface mount connection]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to have the components be mounted in the same surface mounting manner of Uchikoba in the device of Fukuoka and Uchida, in order to simplify the manufacturing process and make the overall device more reliable since wire bonds are known to be quite fragile and subject to disconnection.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Ma et al. (US 6,673,697).

Regarding claim 6, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not show wherein at least one chip component comprises a resonator that operates with bulk acoustic waves. Ma et al. does show in Figure 1, wherein at least one chip component comprises a resonator [bulk film resonator 32] that operates with bulk acoustic waves and is surface mountable. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a surface mountable bulk acoustic wave device of Ma on the substrate of

Fukuoka and Uchida, in order to further provide components necessary for a high frequency filter.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Li (US 6,713,860).

Regarding claim 7, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not disclose wherein the at least one chip component comprises a microwave ceramic filter. Li discloses in Figure 5, the use of a ceramic capacitor [506, column 13, lines 52-60] that is surface mounted on a multilayer substrate [502]. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to (1) have a ceramic capacitor of Li in a microwave ceramic filter and (2) have a microwave ceramic filter on the substrate of Fukuoka and Uchida, in order to provide components necessary for the operation of a microwave frequency ceramic filter.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Asahi et al. (US 6,955,948).

Regarding claim 8, Fukuoka and Uchida disclose the electronic component of claim 1, and that it contains inductors, capacitors, and resistors [column 13, lines 55-65]. Fukuoka and Uchida do not specifically disclose a LC chip filter. Asahi et al. discloses the at least one chip component comprises an inductive-capacitive (LC) chip filter [column 9: lines 10-17]. It would have been obvious to one of ordinary skill in the

art at the time the invention was made to use a LC filter in a high frequency circuit used in receiving and transmitting circuits. The ordinary artisan would have been motivated to use the LC filter in the invention of Fukuoka and Uchida as suggested by Asahi to provide the necessary filtering, modulation, and various other signal shaping functions necessary to the task.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Figueroa et al. (US 6,388,207).

Regarding claim 9, Fukuoka and Uchida disclose the electronic component of claim 1. Fukuoka and Uchida do not show a stripline filter. Figueroa et al. discloses the at least one chip component comprises a stripline filter [capacitor used as signal filter to deliver improved signal integrity through the substrate to the semiconductor chips, disclosed in column 3: lines 24-34, column 4: lines 1-10, and column 6: lines 24-34]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a stripline filter of Figueroa in the substrate of Fukuoka and Uchida, in order to improve the signal quality being fed through the substrate to the supported electronic component.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Uchikoba (US 6,628,178) in further view of Liu et al. (US 6,060,954).

Regarding claim 14, Fukuoka, Uchida, and Uchikoba disclose the electronic component of claim 13. Fukuoka, Uchida, and Uchikoba do not show wherein the at

least part of an adjustment circuit integrated in the multi-layer substrate is formed as one or more strip conductors on the upper side of the multi-layer substrate. Liu et al. do disclose in Figure 2B and 2F, wherein the at least part of an adjustment circuit [column 2, lines 40-45] integrated in the multi-layer substrate is formed as one or more strip conductors [101] on the upper side of the multi-layer substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a stripline conductor of Liu on the upper surface of the substrate of Fukuoka, Uchida, and Uchikoba, in order to allow for the re-workability of the circuit and simplify the fabrication process with respect to the substrate, rather than burying the conductors, making vias, and bonding pads.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Harper (*Electronic Packaging and Interconnection Handbook*).

Regarding claim 17, Fukuoka discloses the electronic component of claim 1. Fukuoka does not disclose the details of the composition of the ceramic used wherein the multi-layer substrate comprises layers of Silicon and Silicon Oxide. Harper discloses the use of SiO2 in packaging ceramics [Table1.16, Page 1.59]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a use the SiO2 as taught by Harper as the main constituent of the ceramic material of Fukuoka in order to provide a material which is less subject than many other ceramics, to the effects of thermal expansion which can severely reduce the reliability of the overall device.

Regarding claim 18, Fukuoka discloses the electronic component of claim 1. Fukuoka does not specify wherein the multi-layer substrate comprises one or more layers of an organic material. Harper does disclose wherein packaging ceramics could be of an organic material, like SiC or Silicon Carbide [Table 1.16, Page 1.59]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a use the SiC as taught by Harper as the main constituent of the ceramic material of Fukuoka in order to provide a material which is highly thermally conductive and is suitable as a substrate for devices which require stringent thermal considerations.

Claims 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US 5,818,699) in view of Uchida et al. (US 5,889,325) in further view of Juskey et al. (US 6,356,453).

Regarding claim 29, Fukuoka and Uchida disclose the method of claim 27. Fukuoka and Uchida do not show wherein the at least one chip component and/or the at least one discrete circuit element is mechanically stabilized using a casting compound. Juskey et al. do disclose in Figure 5, wherein the at least one chip [522] component and/or the at least one discrete circuit element [536] is mechanically stabilized using a casting compound [536]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a casting compound as taught by Juskey in the package of Fukuoka and Uchida in order to provide a material which protects the electronic components from the ambient environment.

Response to Arguments

Applicant's arguments with respect to claims 1 and 26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571) 272-8797. The examiner can normally be reached on M-F, 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eduardo A. Rodela
Examiner ER